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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,394	12/28/2001	Seong-jae Lee	2013p006	8538

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n N .	Applicant(s)	
	10/033,394	LEE ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sh t with the correspondenc address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7-12 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7-12 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1, 4-5, 7-12, and 15-20 have been considered but are moot in view of the new ground(s) of rejection.

New Grounds of Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Allman et al. (U.S. Patent 5,340,770).

In re claim 1, **Allman** discloses a method of fabricating an integrated circuit comprising (col. 2, line 23 to col. 4, line 14 and **FIGS. 1-4**): forming a diffusion barrier layer pattern on a semiconductor substrate **(FIG. 1: 12)** by spin-coating **(FIG. 4: 62)** and densifying **(FIG. 4: 74)** a liquid silicate glass including one of P, As, and B doping elements (col. 2, lines 23-34); forming a SOG layer **(FIG. 1: 14 and 16)** containing impurities, including either one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor substrate (col. 2, lines 23-52); additionally implanting impurity ions into portions of the SOG layer formed on the diffusion barrier layer and the semiconductor substrate to increase the concentration of impurities in the SOG layer (col.

2, lines 23-39); and diffusing the impurity ions contained in the SOG layer having the increased concentration of impurities into the semiconductor substrate by a solid phase diffusion method (col. 3, lines 30-35) to form shallow junctions (col. 4, lines 3-5).

In re claim 7, **Allman** discloses wherein the shallow junctions are formed by the solid phase diffusion method using one of rapid thermal annealing (RTA), spike annealing, and laser annealing (col. 3, lines 31-36 and **FIGS. 3-4**).

In re claim 8, **Allman** discloses wherein in the RTA, the semiconductor substrate on which the SOG layer having the increased concentration of impurities is formed is rapidly thermally annealed in an inert gas atmosphere (col. 3, lines 24-36).

2. Claims 11, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Allman et al. (U.S. Patent 5,340,770).

In re claim 11, **Allman** discloses a method of fabricating an integrated circuit comprising (col. 2, line 23 to col. 4, line 14 and **FIGS. 1-4**): forming a gate pattern (col. 2, lines 24-34 and **FIG. 1**) on a semiconductor substrate **(Fig. 1: 12)**; forming a SOG layer **(FIG. 1: 14 and 16)** containing impurities, including either one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor substrate (col. 2, lines 23-52) by spin-coating **(FIG. 4: 62)** and densifying **(FIG. 4: 74)** a liquid silicate glass including one of P, As, and B doping elements (col. 2, lines 23-34); additionally implanting impurity ions into portions of the SOG layer formed on the gate pattern and the semiconductor substrate increase the concentration of impurities in the SOG layer (col. 2, lines 23-39); and diffusing the impurity ions contained in the SOG layer into the semiconductor substrate by a solid phase diffusion method (col. 3, lines 30-35) to form

shallow junctions (col. 4, lines 3-5) having a LDD region self-aligned underneath both sidewalls of the gate pattern and a highly doped source/drain regions adjacent to the LDD region **(FIGS. 1-4)**.

In re claim 17, **Allman** discloses wherein the shallow junctions are formed by the solid phase diffusion method using one of rapid thermal annealing (RTA), spike annealing, and laser annealing (col. 3, lines 31-36 and **FIGS. 3-4**).

In re claim 18, **Allman** discloses wherein in the RTA, the semiconductor substrate on which the SOG layer having the increased concentration of impurities is formed is rapidly thermally annealed in an inert gas atmosphere (col. 3, lines 24-36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 5, 8, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allman et al. (U.S. Patent 5,340,770) as applied to claims 1, 7, and 8 above, and further in view of Kroner et al. (IEEE 2000).

In re claim 4, **Allman** does not explicitly disclose wherein the concentration of impurities of the SOG layer is increased using a plasma ion implanter including a Plasma Immersion Ion Implanter (PIII) and an Ion Shower Implanter (ISI).

Kroner et al. disclose (page 476) wherein the concentration of impurities of a layer is increased by using a plasma ion implanter including an Ion Shower Implanter

(ISI) and Plasma Immersion Ion Implanter (PIII). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Allman and Kroner to enable the process of additionally implanting impurity ions into portions of the SOG layer of Allmand to be formed furthermore to it is a doping method for high dose and low energy implants (page 476, Abstract).

In re claims 5, 8, 9, and 10, **Allman** does not explicitly disclose the ranges for the maximum impurity implantation concentration, the rapidly thermally annealed temperature of the SOG layer, and the doping depth and doping concentration of the shallow junctions.

However, there is no evidence indicating that the ranges for the maximum impurity implantation concentration, the rapidly thermally annealed temperature of the SOG layer, and the doping depth and doping concentration of the shallow junctions is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP§2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

4. Claims 12, 15, 16, 18, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allman et al. (U.S. Patent 5,340,770) as applied to claims 11, 17, and 18 above, and further in view of Kroner et al. (IEEE 2000).

In re claim 15, **Allman** does not explicitly disclose wherein the concentration of impurities of the SOG layer is increased using a plasma ion implanter including a Plasma Immersion Ion Implanter (PIII) and an Ion Shower Implanter (ISI).

Kroner et al. disclose (page 476) wherein the concentration of impurities of a layer is increased by using a plasma ion implanter including an Ion Shower Implanter (ISI) and Plasma Immersion Ion Implanter (PIII). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Allman and Kroner to enable the process of additionally implanting impurity ions into portions of the SOG layer of Allmand to be formed furthermore to it is a doping method for high dose and low energy implants (page 476, Abstract).

In re claims 12, 16, 18, 19, and 20, **Allman** does not explicitly disclose the ranges for ratio thickness, the maximum impurity implantation concentration, the rapidly thermally annealed temperature of the SOG layer, and the doping depth and doping concentration of the shallow junctions.

However, there is no evidence indicating that the ranges for ratio thickness, the maximum impurity implantation concentration, the rapidly thermally annealed temperature of the SOG layer, and the doping depth and doping concentration of the shallow junctions is critical and it has been held that it is not inventive to discover the

optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation.

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1, 4-5, 7-12, and 15-20 have been considered but are moot in view of the new ground(s) of rejection.

In response to Applicants' argument that, "Applicants must disagree with the Examiner's contention since the cited passage contains no reference to forming of the SOG layer by spin-coating and densifying a liquid silicate glass including one of P, B, In, As, and Sb doping elements as required by Claims 1 and 11", examiner respectfully disagree. Since Applicants' amendment necessitated the new ground(s) of rejection presented in this Office Action. Applicants are directed to page 3, 2nd paragraph of the present Office Action, where the newly discovered reference, Allman et al. (U.S. Patent 5,340,770) discloses a method of fabricating an integrated circuit comprising (col. 2, line 23 to col. 4, line 14 and **FIGS. 1-4**): forming a gate pattern (col. 2, lines 24-34 and **FIG. 1**) on a semiconductor substrate **(Fig. 1: 12)**; forming a SOG layer **(FIG. 1: 14 and 16)** containing impurities, including either one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor substrate (col. 2, lines 23-52) by spin-coating **(FIG. 4: 62)** and densifying **(FIG. 4: 74)** a liquid silicate glass including one of P, As, and B doping elements (col. 2, lines 23-34); additionally implanting impurity ions into portions of the SOG layer formed on the gate pattern and the semiconductor substrate increase the concentration of impurities in the SOG layer (col. 2, lines 23-39); and

diffusing the impurity ions contained in the SOG layer into the semiconductor substrate by a solid phase diffusion method (col. 3, lines 30-35) to form shallow junctions (col. 4, lines 3-5) having a LDD region self-aligned underneath both sidewalls of the gate pattern and a highly doped source/drain regions adjacent to the LDD region **(FIGS. 1-4)**.

For these reasons, the new ground(s) of rejection is considered proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
April 15, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER